REMARKS

In the Office Action, the Examiner objected to the specification because the specification included hyperlinks. In the response to the previous Office Action, the specification was amended to remove the hyperlinks. Applicants request that the Examiner point out the location of the hyperlinks in the amended specification or withdraw the objection.

Applicants note that the claim number 47 was repeated in the original claims. The claims were renumbered in the response to the previous Office Action to remove the typographical error. Applicants affirm the provisional election to prosecute claims 1-18, 24-29, and 32-48 made in response to the Examiner's restriction requirement. Thus, claims 1-18, 24-29, and 32-48 are pending in the present application. In the Office Action, the Examiner indicated that claims 40-47 are allowed. In view of the aforementioned typographical error, Applicants believe that claims 40-48 are allowed.

Applicants note that the Examiner has provided contrary indications as to the disposition of some of the pending claims in the Office Action Summary and the Detailed Action. The following summary represents Applicants understanding of the current disposition of the pending claims. In the Office Action, claims 1-3, 6-8, 11-18, 24, 25, 27-29, 32, 33, and 35-38 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Lindsay, et al (U.S. Patent Publication No. 2002/0194415). Claim 5 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay in view of any one of Hwang (U.S. Patent No. 6,516,398), Ma, et al (U.S. Patent No. 6,182,235), or Dea, et al (U.S. Patent No. 5,742,833). Claim 9 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lindsay in view of admitted prior art. The Examiner's rejections are respectfully traversed.

Independent claims 1, 24, 32, and 35 set forth, among other things, an integrated circuit configured as a bridge. The integrated circuit includes an internal bus, a microcontroller connected to the internal bus, and an Ethernet controller coupled to the internal bus. A plurality of buffers is coupled between the microcontroller and the Ethernet controller for buffering the data. For example, the Ethernet controller 344 is coupled to an ASF receive buffer 328, which is in turn coupled to the MC A/D bus 322. The microcontroller 320 is also coupled to the MC A/D bus 322. See Patent Application, Figure 4 and related discussion in the specification.

Lindsay describes an integrated Ethernet controller 800 that includes an alert supervisory bus controller 825 and a media access controller 808 that are coupled to an internal bus 811. A buffer memory 818 is also coupled to the internal bus 811. However, the buffer memory 818 is not coupled between the alert supervisory bus controller 825 and the media access controller 808. Thus, Applicants respectfully submit that Lindsay fails to describe or suggest a plurality of buffers coupled between a microcontroller and an Ethernet controller, as set forth in independent claims 1, 24, 32, and 35. For at least this reason, Applicants respectfully submit that claims 1-3, 6-8, 11-18, 24, 25, 27-29, 32, 33, and 35-38 are not anticipated by Lindsay.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the cited references. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Lindsay fails to describe or suggest a plurality of buffers that are coupled between a microcontroller and an Ethernet controller, as set forth in independent claims 1, 24, 32, and 35. The Examiner relies on a number of secondary references to teach an embedded 8051 microcontroller. The Examiner also relies

upon the admitted prior art to teach a south bridge. However, none of the secondary references remedy the fundamental deficiency of the primary reference.

Lindsay also teaches away from Applicants' claimed invention. In particular, Lindsay teaches that the alert supervisory bus controller 825, the media access controller 808, and the buffer memory 818 should all be coupled to the internal bus 811 so that all of these devices may have direct access to the internal bus 811. Thus, Lindsay teaches away from a plurality of buffers that are coupled between a microcontroller and an Ethernet controller, as set forth in independent claims 1, 24, 32, and 35. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

Thus, for at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case that the present invention is obvious over the cited references and request that the Examiner's rejections of claims 5 and 9 under 35 U.S.C. § 103(a) be withdrawn.

In the Office Action, the Examiner objected to claims 4, 10, 26, 34, and 39 as being dependent upon a rejected base claim, but indicated that these claims include allowable subject matter. In view of the above arguments, Applicants respectfully submit that independent claims 1, 24, 32, and 35 are in condition for allowance and therefore dependent claims 4, 10, 26, 34, and 39 are also allowable for at least the reasons discussed above. Applicants request that the Examiner's objections to these claims be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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